AMENDMENTS TO THE SPECIFICATION

Please amend the specification as below. A clean copy of the amended specification is provided as a separate attachment to this response.

[0001] This invention relates generally to the fabrication and testing of semiconductor wafers having discrete semiconductor ~~dice~~ dies. More specifically, the present invention relates to methods of temporarily isolating semiconductor ~~dice~~ dies from a common conductor during wafer level testing.

[0002] In semiconductor manufacture, a large number of often complex electrical devices, also known as ~~dice~~ dies or integrated circuit (IC) chips, are fabricated on a semiconductor wafer. After fabrication, the ~~dice~~ dies are subjected to a series of test procedures prior to wafer dicing and packaging to assess the electrical characteristics of the circuitry of each. ~~Dice~~ Dies which are determined to meet specifications are allowed to continue in the manufacturing process. Those which do not meet specifications are removed from the manufacturing process.

[0003] One series of testing is known as a "wafer level test," which applies stress conditions to the ~~dice~~ dies on the wafer in an effort to accelerate certain types of failures. Wafer level testing may involve elevated voltage, elevated temperature,

elevated humidity or any other condition which a manufacturer deems appropriate to expose failures which can be detected using test equipment.

[0004] To facilitate wafer level testing, a common conductor, e.g., a buss, may be provided which interfaces a plurality of ~~dice~~ dies under test such that a signal is propagated to the plurality of ~~dice~~ dies simultaneously. One exemplary common conductor may, for example, connect individual die power inputs to a common power source, e.g., Vcc, Vss. Other common conductors may be used to supply other signals in common to the ~~dice~~ dies under test.

[0005] The use of a common conductor to supply a signal to multiple ~~dice~~ dies has its drawbacks. When a die is found to be defective, the defective die must be isolated from the common conductor(s) so that non-defective ~~dice~~ dies are not affected by electrical conditions occurring at the defective die.

[0012] Figure 3 shows a simplified process sequence for isolating and testing ~~dice~~ dies using the Fig. 1 or Fig. 2 embodiment of the invention;

[0021] The invention provides the capability to perform wafer level testing while temporarily isolating a die for testing from other ~~dice~~ dies which are otherwise in electrical communication with a common conductor. In the invention, at least one temporary isolation device is provided between each die and a common conductor to

temporarily electrically isolate the die from the common conductor. The temporary isolation device may be a diode, transistor or other element. When a diode is used it can be reverse biased such that the individual die is isolated from the common conductor. The invention also provides a temporary isolation testing system and procedure which is compatible with conventional test equipment already in use.

[0024] Also, for simplicity, a common conductor will be discussed below as one or more power supply conductors; however, the common conductor can be used to supply any signal to plural ~~dice~~ dies connected to it.

[0025] The invention will now be explained with reference to Figs. 1-10. Fig. 1 discloses one exemplary embodiment of the invention. A portion of a wafer is shown as containing a plurality of ~~dice~~ dies 5 which are to be tested before die singulation. A common conductor 1 is provided on the wafer and is used to supply a first signal, for example, a positive Vcc voltage, to the individual ~~dice~~ dies. Likewise, a common conductor 3 is provided on the wafer and is used to supply a second signal, for example, a Vss voltage (ground), to the individual ~~dice~~ dies.

[0025] A plurality of probe pads 13 are provided in direct electrical communication to another common conductor 3 each in proximity to a die 5 on the wafer. A probe pad 15 resides on each die 5 in proximity to the closest probe pad 13 on the wafer. A permanent isolation device 7 (e.g. fuse) may be interposed between each

probe pad 13 and a probe pad 15. A probe pad 21 is provided on each die 5 and is connected to, for example, the normal Vss voltage input terminal of the die. A temporary isolation device 19 (e.g. diode) is installed on the die 5 between each probe pad 21 and probe pad 15. The diode 19 is installed such that it is operative in a forward bias manner during wafer level testing allowing a signal to pass between probe pad 21 and probe pad 15. When temporary isolation is needed, the diode 19 is reverse biased thereby isolating the die 5 from the common conductor 3. It should be recognized that while Fig. 1 shows a permanent isolation device 7 (e.g. fuse) and a temporary isolation device 19 (e.g. diode) interposed between each common conductor and the die, it may be desirable to also have some common conductors which are connected directly to the ~~dice~~ dies 5 without interposed permanent or temporary isolation devices. Also, although Fig. 1 shows the permanent isolation devices 7 fabricated on the wafer off the ~~dice~~ dies 5 and the temporary isolation devices 19 fabricated on the ~~dice~~ dies, it is possible to fabricate both off the ~~dice~~ dies 5 or both on the ~~dice~~ dies 5, or with the temporary isolation device 19 off the ~~dice~~ dies 5 and the permanent isolation device 7 on the ~~dice~~ dies. It is also possible to provide the common conductor on an external interface, e.g. a test head or a probe card, and provide one or both of the permanent isolation device 7 and temporary isolation device 19 on the external interface.

[0026] The common conductors 1 and 3 may supply any signals necessary for die operation or testing and thus, as noted, are not limited to supplying first and second voltage signals, e.g. Vcc and Vss. The common conductor may be a single conductor or may be part of a group of common conductors which provide signals to the ~~dice~~ dies 5.

[0029] As can be seen in Fig. 1, when the diodes 19 between pads 11 and 17 and pads 21 and 15 are reverse biased during probe testing procedures of an individual die, only a small amount of leakage will be observed passing to the common wafer conductors 1 and 3 through the permanent isolation device, e.g. fuse 7. Accordingly, each die may be individually tested with a first and second signal, e.g. Vcc and Vss respectively provided through probe pads 17 and 21, without affecting other ~~dice~~ dies connected to the common conductors 1 and 3. If during such individual testing a die is found to be defective, the permanent isolation device 7 associated with the defective die may be used by means well known in the art (e.g. fuse blowing) to permanently isolate the die from the common conductors 1 and 3 thereby enabling the common conductors to effectively power the serviceable ~~dice~~ dies during wafer level testing procedures.

[0030] Fig. 1 shows the permanent isolation device 7, e.g., fuse, provided on a wafer and off the ~~dice~~ dies 5 and between pads 9 and 11 and between pads 13 and 15. However, as noted, the permanent isolation device can be provided at other locations,

including on each die 5, or on an external interface, between a common conductor 1 and a die signal pad on the die requiring a signal from the common conductor. Moreover, the temporary isolation devices 19, e.g., diodes, may be directly connected to a respective common conductor, e.g. 1, 3 with the permanent isolation devices being connected between the temporary isolation devices and die.

[0032] Fig. 3 shows a simplified processing sequence used for testing each die 5 in Fig. 1. First, in processing segment 101, single die level signals are applied from an external interface to the pads 17 and 11 and 21 and 15 to supply signals to the temporary isolation device(s). Other probes of the external interface may be applied to other signal pads of each die 5 during testing. This reverse biases the diodes used as temporary isolation devices 19, thereby isolating a die 5 from the common conductors 1 and 3. In processing segment 103, testing of an isolated die 5 is performed. If the testing reveals that a die 5 should be permanently isolated, then in processing segment 105, the permanent isolation devices 7 are activated, e.g., fuses blown, to permanently isolate defective ~~dice~~ dies 5 from the common conductors 1, 3. As shown in processing sequence 107, when the wafer is subjected to wafer level testing conditions, including, for example, wafer level burn-in, signals are applied to conductors 1, 3 which during operation forward bias the diodes 19, permitting common conductors to supply desired

signals to all dies still connected to the common conductors. Tests are then conducted with all ~~dice~~ dies 5 receiving common signals from the common conductors.

[0033] The processing sequence of Fig. 3 may be varied from that shown to perform testing or other operations which require temporary isolation of ~~dice~~ dies 5 from one or more common conductors. For example, die isolation and individual die testing using the Fig. 1 embodiment, may be accomplished after signals are commonly applied to all ~~dice~~ dies through the common conductors 1 and 3 (segment 107). The permanent isolation devices 7, e.g. fuses, can be opened, e.g. fuses blown, either automatically or manually when defective ~~dice~~ dies are identified when signals are applied to conductors 1, 3. The permanent isolation devices may also be opened when signals are applied directly to the die pads 17 and 21 and defective device ~~dice~~ dies 5 are found. Permanent isolation devices 7, such as fuses, may be activated by use of any technology which is appropriate for providing permanent isolation of ~~dice~~ dies from a common conductor. When fuses are used, the fuse itself can be automatically blown when excessive current passes through it, or it can be opened by laser, mechanical severance, applying a sufficient high voltage across it, or other technique.

[0042] Also, during temporary isolation, individual ~~dice~~ dies 5 may be tested in a predefined order or simultaneously.